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A 5 GHz, 1.2 dB NF Common Gate Low Noise Amplifier using 30 nm DG-FinFET for Wideband Applications

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Abstract

Objectives: To design a Low Noise Amplifier (LNA) using Double Gate (DG) FinFET with 1.2 dB noise figure over bandwidth of 24GHz. **Methods**: Temperature effect on noise figure, stability is also analyzed and the effect of thermal noise and flicker noise in CG LNA is presented. **Findings:** The designed LNA gives an IIP3 value of 5.58 dB and 1dB compression point of -5.6 dB with proper matching conditions. The maximal efficiency of 80% was achieved for different topologies with 364 MHz switching frequency. **Improvements**: The designed amplifier provides a maximum voltage gain of 17 dB with a noise figure less than 2 dB as compared to that of conventional MOSFETs based LNA.

Keywords: DG-FinFET, IIP3, Low noise Amplifier, Noise Figure, Stability

1. Introduction

Scaling of conventional MOSFET below 45 nm takes some new processing steps or other concepts of devices like FinFETs. In[1] the experiment results and simulations show that, the down scaling of bulk devices below 45 nm still improves the performance in RF application for certain aspects. It is observed that for low frequency, high gain applications Fin FET are better than planar bulk CMOS. The analog device performance of planar transistors and Fin FET are studied in[2]. In those works the analog-RF performance of both devices from low frequency to certain mm frequency range are tested. Fin FET offers a better matching performance but when it deals with frequency it shows an inferior behavior[3]. It is mainly due to the presence of several parasitic elements especially lower mobility and higher resistance along the sidewall which results in the degradation of f_T and f_{max}. When consider the other figure of merits like linearity and noise figure there are no significant difference among the two devices[4]. Beyond all these some studies reveals that Fin FET well suited for low-frequency, low-power RF and analog applications[5,6]. Although Fin FET having advantage over bulk MOSFETs when they come to use in different analog-RF applications they have to deal with many challenges like different types of noises, parasitic effects at high frequency[7]. FinFET have many advantage compared to that of bulk CMOS transistors in terms of better gate control which give rise to reduced short channel effects, less sub threshold performance Fin FET lag behind the planar bulk CMOS devices because of reduced trans conductance due to the higher resistance in the source drain resistance in narrow fin devices and reduction in mobility due to dependency in surface orientation and a higher fringing capacitance[8]. Fin FET doesn't offer much noise and more non linearity than planar devices. In[9] the importance and advantage of Fin FET in the RF field is discussed. The high frequency performance and the effect of parasitic capacitance are studied in details. The application of Fin FET in RF fields are reported in[10,11]. RF receiver design using independent double gate MOSFET is presented in[12]. DG-MOSFET based

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60GHz Low Noise Amplifiers are presented in[13], which the tunability, efficiency and performance are evaluated. There are a few works related Fin FET to 45 nm Fin FET-based RF circuits are overall somewhat inferior compared to planar 90 nm CMOS node versions. In[14] varying different parameters of Fin FET, the impact of speed of Fin FET and the analysis of Fin FET based LNA are studied. The NF is observed about 1.5dB with a gain of 13.5. In[15] design and optimization of ultra-low power low noise amplifier is presented. Using particle swarm optimization, optimized LNA achieves 12.6 dB voltage gains, 3.19 dB noise figures and consumes 869 μ W power. In[16] deals with the design of single-stage differential low-noise amplifiers for Ultra-Wideband (UWB) applications, comparing state-of-the-art planar bulk and Silicon-On-Insulator (SOI) Fin FET CMOS technologies featuring 45 nm gate length. The amplifier amplifiers have been designed to work over the whole UWB band (3.1–10.6 GHz).The effect of gate – drain/source under lap (L_{un}) on a narrow band LNA performance has been studied in 30 nm Fin FET using device and mixed mode simulations[16]. In[17] a CMOS Low Noise Amplifier Design for Low Power Transmission was proposed and results shows a very low noise figure of 1.3 dB with a gain of 9.8 dB and the reflection coefficientis-11.5 dB. The objective of this work is to design of a Low Noise Amplifier using Double Gate Fin FET and a complete analysis of all the performance matrices. In this work we also focus on a detailed analysis of Noise Figure in Fin FET based Common Gate LNA using BSIM-CMG Model and the internal and external parasitic capacitance and resistance effect in Noise Figure. It also proved the design is thermally stable and with less noise figure variation under high temperature.

2. BSIM-CMG Model and Methodology

BSIM-CMG is implemented in Verilog A. It is a surface potential based model, i.e., the I-V and C-V characteristics are expressed in terms of electronic potentials at the silicon/oxide interfaces. It covers all the multi-gate transistor properties. The charges and currents are calculated from surface potential[18] It provides flexibility to model devices. It supports different mode within the models. BSIM-CMG processes scalability with Fin FET related geometry, including parameter such as height and number of fins, smoothness of the model and accurate capacitance. Beyond all, these BSIM-CMG exhibits some other properties such as channel length modulation, mobility degradation, quantum mechanical effects, flicker and thermal noise, noise associated with the device. The version of model used here is BSIM CMG 107.0. The following settings have to be made before simulation with the device. The DEVTYPE = 1 indicate the NMOS type and zero indicate the PMOS type. Geometric mode values for the Fin FET are shown in Table 1. GEOMOD = 0 for Double gate and its value is 1 for TG 2 for QG and so on. Similarly the parasitic capacitance, resistance etc can include in the device by properly setting the values of RDSMOD and CGEOMOD. The steps followed for creating the Fin FET model in cadence is shown in Figure 1. First creating a new library in cadence and the Verilog, a code for the respective models are added up. The models files, noise models, parasitic resistance and capacitance models are also included. While during simulation include the model file for NMOS and PMOS.

3. Common Gate LNA Topology

The common gate and common source topologies are most popular topologies used in Low noise amplifier which may applicable in different receiver. Both of these topologies meet all the requirements of narrow band LNA design. In the case of common source topology, inductive degeneration helps to achieve better impedance matching with less noise effects. As we consider the common gate LNA topology, which is having better linearity, isolation property and inherent wideband applications[19]. But

Table 1. Bsim-CMG parameters

Parameter	Nominal value
Gate Length	30nm
W_{eff}	10μm
Effective Oxide thickness	1nm
Channel Doping	$1x10^{16}/cm^3$
FiPitch(FPITCH)	80nm
Body (fin) thickness (TFIN)	15nm
I_{min}	1FA

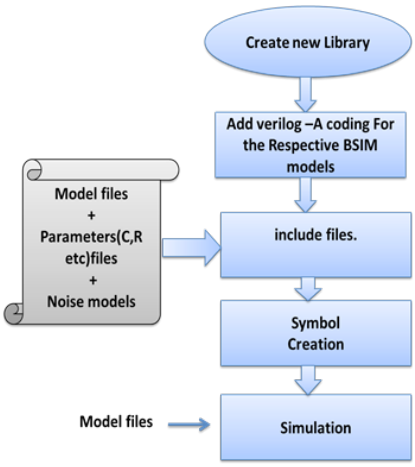


Figure 1. Simulation using BSIM-CMG model.

as we goes for higher frequency application the effect of parasitic capacitance of operating transistor degrade the performance. In the case of Fin FET and other multi gate transistors this effects will be prominent and the introduction of parasitic elements creates many problem. The typical CG LNA topology is shown in Figure 2.

In the case of a typical CG LNA the input impedance is given as

$$Z_{in}=\frac{1}{g_m + X_c} \quad (1)$$

Where X_c is the impedance offered by the parasitic capacitance and other capacitance associated with the device, which is also a function of $C_{gs.}$ Thus it can be also defined as

$$Z_{in}=\frac{1}{g_m + j\omega C_{gs}} \quad (2)$$

In the case of CMOS the effect will be less, but as we move to multi-gate devices the effect will be more predominant especially at high frequency[20]. But in some cases of Low noise amplifier and power amplifier with multi-gate devices like Fin FET, without use any inductors and all we can get the impedance matching with non-quasi-static effects of channel resistance due to finite charging of carriers in the channel[21]. As the operating frequency gets increases C_{gs} comes in action, which degrades the whole performance of the amplifier. The introduction of a shunt inductor at the input side helps to achieve a better impedance match since it forms the resonance condition with the C_{gs}. When we compare CS LNA with CG LNA it is noticed that CG LNA a better stability and good reverse isolation since the lack of C_{gd} path in CG LNA.

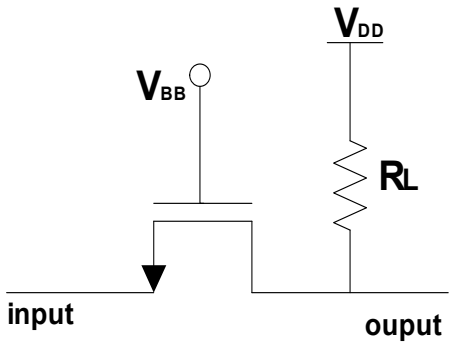


Figure 2. Typical CMOS common gate LNA.

3.1 Circuit Analysis and Design

The circuit shown in Figure 3 is for a single ended common gate low noise amplifier. At the input node the bonding pad is included, during simulation it provide the real parasitic capacitance effect at the input node. The Fin FET biased in such a way that it will provide a maximum value of g_m at V_{bias} of 470 mv and g_m of 20 mA/V the circuit having a source impedance of 50 Ω. For a better noise performance, the source inductance L_s is used and its value is adjusted in such a way that it will provide a better noise performance. The source inductance L_s and the parasitic capacitance of the source node create a parallel LC resonator. In this design the BSIM-CMG model consists of two gates and a common bias voltage is applied so that the device in saturation region, with a drain current of 1.5 mA-3mA range. The cut-off frequency (f_T) and maximum oscillation frequency (f_{max}) are the most important RF figure merit parameters [Raskin-2006]. These parameters can be calculated from the small signal equivalent circuits.

The cut–off frequency is given by the equation

$$f_t=\frac{g_m}{2\pi C_{gg}} \quad (3)$$

Where g_m is the trans-conductance of the device and C_{gg} is a combination of C_{gs}, $C_{gd,}$ overlap capacitance and fringe capacitance. The f_t value is above 250GHz range. The inductance provided at the source resonates with the source capacitor C_t, which is sum of parasitic capacitance and gate to source capacitance.

$$C_t=C_{gs}+C_{para} \quad (4)$$

The resonance condition is given as

$$Wo=\frac{1}{\sqrt{L_s C_t}} \quad (5)$$

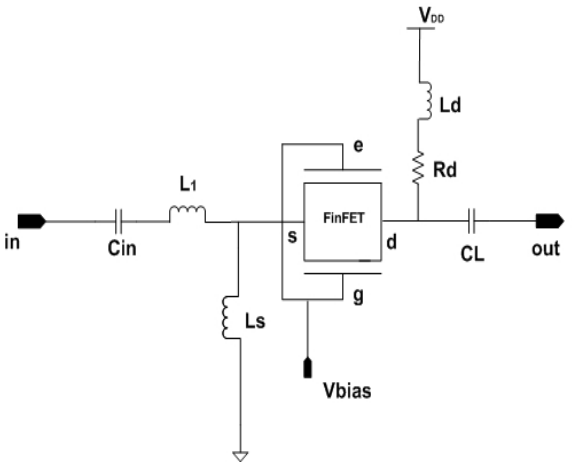


Figure 3. FinFET based CG single ended low noise amplifier at 5GHz with V_{bias} = 470 mv, L_g = 3nH, L_d = 1 nH at 0.9 V.

For an operating frequency of 5GHz the L_s values is obtained in the range of 3-5nH. The inductance values are chosen according to that needed for an on-chip inductor. For this value of inductance the bias voltage is varied from 0 to 0.9V and the width of the transistor is varied such that the g_m = 20 mA/V.

As we know the antenna resistance is R_{in} = 50 Ω, we have

$$g_m = 1/R_{in} \quad (6)$$

or R_{in} = 1/(20 mA/V)

The resistance R_d is provided for low frequency gain and is set in a range for few 200-450 Ω.

The drain inductance value is varied from 1 nH to 5 nH to obtain a good gain and inductance as selected in such a way that all must be on chip.

4. Results and Discussion

Periodic steady state Analysis has been carried out in Cadence Virtuoso (ADE) in order to obtain the required characteristics. Number of harmonics has been varied from 0 to 25 GHz for getting the desired responses. The parameter such as voltage gain, power gain, noise figure, linearity-1 dB comression point and IIP3, dc power are analyzed and simulation results are presented in the following section.

4.1 Noise Figure-NF

Noise figure is one of the important parameters in the aspects of LNA design for CMOS LNA is noticed that CG LNA having a noise figure, NF > 3dB. For Design explained above the NF analysis done and it is observed that by using Fin FET in CG LNA, NF is less than 2 dB from 1.8 GHz to 24 GHZ. The designed frequency, 5GHz lies between this range and it is observed that the NF = 1.26 dB which is very less as compared with the recent CG LNA[22,23]. The noise figure has been found to be increasing well above 5 dB with frequencies above 25 GHz.

The intrinsic noise performance is calculated by the following approximated expression by Ziel equations.

$$F_{min} = 1 + 2(f/f_t)\sqrt{(\gamma\beta(1 - |Im(C)|^2/5)} \quad (7)$$

Where β is the gate excess noise factor, γ drain excess noise factor and *Im(C)* is the imaginary part of the correlation coefficient[24]. The range of β, γ and *Im(C)* of double gate MOSFET are explained and it is observed by substituting the proper values in the above equation we will get the noise Figure below 2dB.BSIM-CMG model is flexible to operate at different parasitic capacitance mode and resistance mode, and its values can be set by giving different values to CGEOMOD and RDSMOD[25]. CGEOMOD mode gives different parasitic capacitance model by setting its values 0, 1, 2. In CGEOMOD = 0 the fringing and overlap capacitance are comes in picture and are proportional to number of fins and effective width of the Fin FET.

Gate to Source fringe capacitance.

$$C_{gs.fr} = NFIN_{total.} W_{eff,CVO}. CFS_i \quad (8)$$

Gate to drain fringe capacitance,

$$C_{gd.fr} = NFIN_{total.} W_{eff,CVO}.CFD_i \quad (9)$$

Where $NFIN_{total}$ is the total number of fins, $W_{eff, CVO}$ is the effective width of constant gate to drain overlap capacitance, CFS_i and CFD_i is the source-side and drain side outer fringe capacitances. In CGEOMOD = 1, which enables the parameters COVS, COVD, CGSP, and CGDP[26] will include in the model. COVS and COVD is constant gate to source and gate to drain overlap capacitance, similarly CGSP and CGDP are the Constant gate to source and gate to drain fringe capacitances. In CGEOMOD = 2 an outer fringe capacitance model for variability modeling which address the complex dependencies on the Fin FET geometry[27] will be invoked. Similarly for different resistance modes RDSMOD = 0,1 also NF of CG LNA is tested is shown in Figure 4 and Figure 5 RDSMOD implies bias-dependent, source/drain

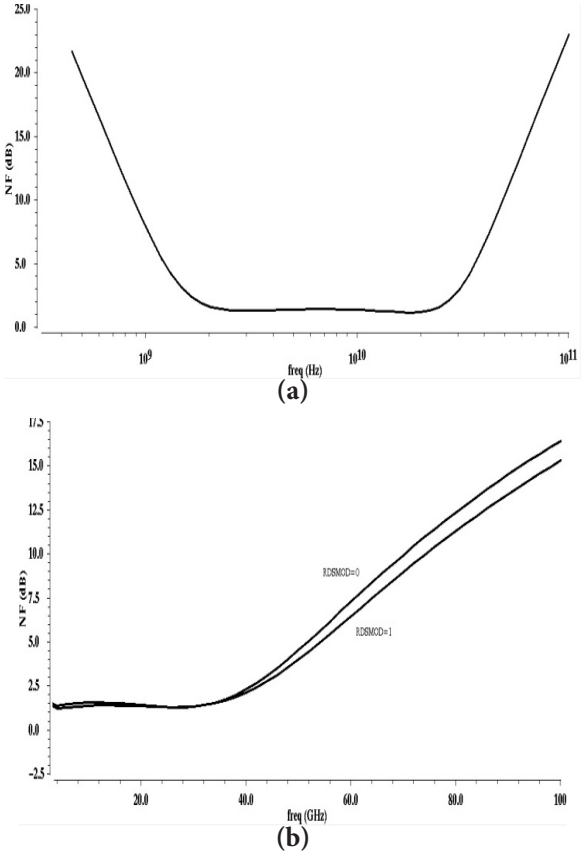


Figure 4. NFR of. **(a)** Common gate low noise amplifier. **(b)** CG with different resistance mode RDSMOD = 0 and RDSMOD = 1.

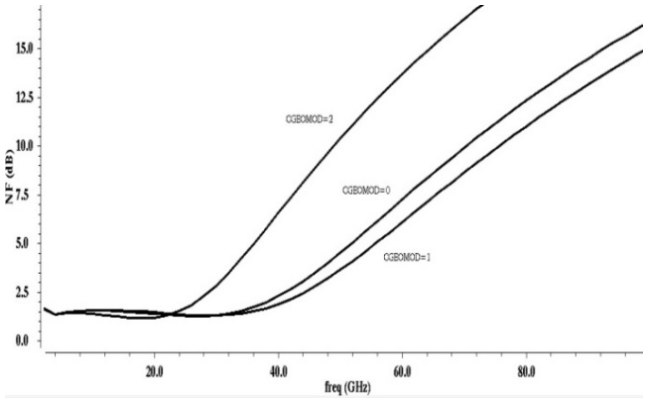


Figure 5. NF Response of CG LNA with different capacitance mode.

extension resistance model selector. The internal Rds (V) option can be invoked by setting the model selector RDSMOD = 0 (internal) and the external one for Rs(V) and Rd(V) by setting RDSMOD = 1.

4.2 Temperature Effect on Noise Figure

Noise Figure Analysis of CG LNA is done from 500 MHz to 100 GHz and it is observed[28] that noise Figure is below 2 db from 1.8 GHz to 24 GHz at room temperature. Temperature is varied from 20°C to 80°C. It is observed that up to 50°C the noise figure response with frequency doesn't show much difference. As we goes on increase the temperature there is a slight variation in noise figure i.e., a variation of 2 dB nearly at 80°C and then it remains constant[29]. Noise Figure Variation is about 0.5 dB from a temperature of 20°C to 80°C. Above 50°C further increase of temperature Noise Figure remains constant as shown in Figure 6.

4.3 Thermal and Flicker Noise Effect on Noise Figure

We know that noise Figure

$$NF = 10\log(F) = 10\log(SNR_{in} / SNR_{out}) = SNR_{in,dB} - SNR_{out,dB} \quad (10)$$

Where SNR_{in} and SNR_{out} are the input and output signal to noise ratios.

The noise figure is the noise factor, given in dB

$$NF = 10\log(F) \quad (11)$$

Noise Temperature is one way of expressing the level of available noise power introduced by a component or source. The noise temperature of amplifiers refers to the noise that would be added at the amplifier's input. The effect of thermal noise and flicker noise on CG LNA is studied. It is observed that the noise figure response is almost follow the same response from 2 GHz to 30 GHz .At high frequency range, i.e., above 30 GHz the thermal noise effect is predominant. Flicker noise doesn't

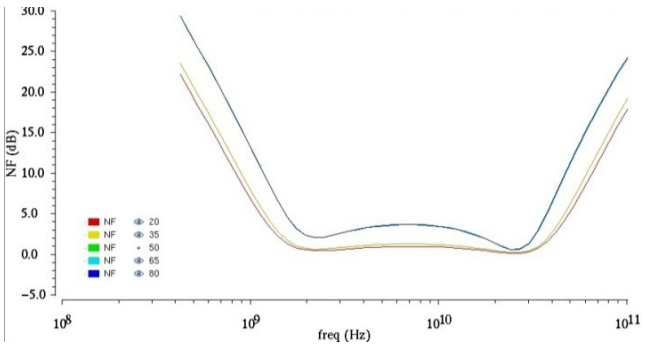


Figure 6. Noise figure vs frequency response.NF = 1.26 dB at 5 GHz.

have much effect on the noise figure response in this design. The Figure 7 indicates the spot Noise summary of the CG LNA at 5 GHZ. The Pie chart of spot noise indicated in Figure 7 shows how much noise contributed by the components of the design. It is clear that the noise contribution from the device side is too less, it is only about 8.47% out of the whole noise contributed by the design and it is of thermal noise. Effect of thermal noise is mainly due to the parasitic assessing of resistance. The flicker noise effect is mainly occurs in the low frequency region and the effect of flicker noise 5 GHz range is negligible. In Figure 8 the red colored plot represent the Noise Figure Response without thermal noise effect and the blue colored plot represent the Noise Figure effect with thermal noise. At 5GHz, the operating frequency Noise Figure variation is very less about .7 dB and above 30 GHz Noise Figure variation is more due to the effect of Flicker noise in addition to thermal noise.

4.4 Voltage Gain

The transient response for the CG LNA using Fin FET is shown in Figure 9. Input signal of 5 mV peak to peak is given at the input at 5 GHz and it is observed that amplified output at the output with a peak to peak value of 35 mV.

Thus the voltage gain in dB obtained as

$$Av = \frac{20 \log V_{out}}{V_{in}} \quad (11)$$

Av = 16.9 dB

The voltage gain spectrum at different frequencies is shown in Figure 10. It is observed that at 5 GHz the gain is maximum and is equals to 17 dB, gain got decreases and increase in frequency.

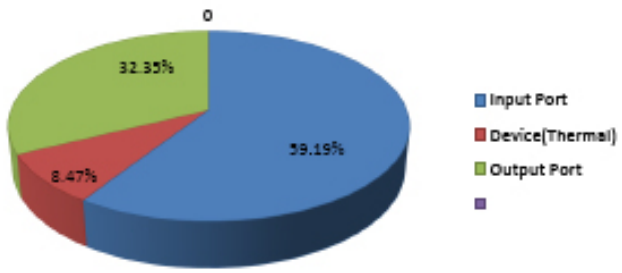


Figure 7. Spot noise summary of the CG LNA at 5 GHZ.

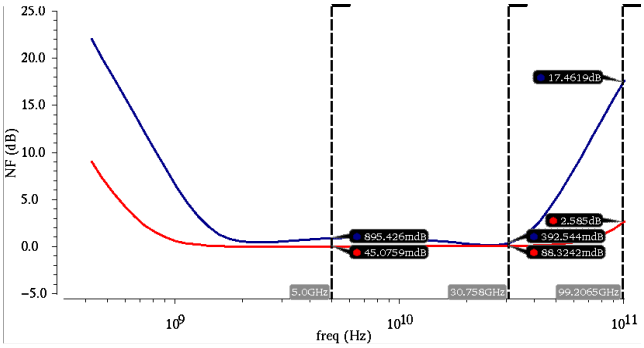


Figure 8. Thermal noise effect vs Frequency plot.

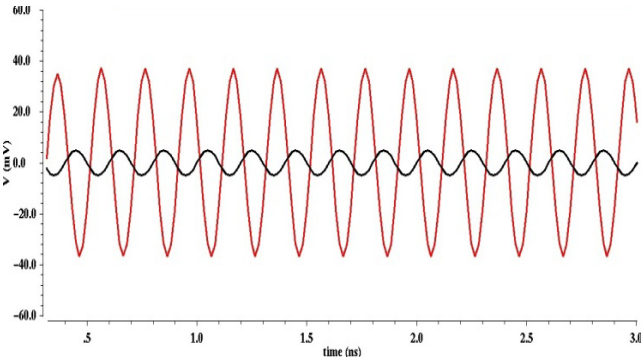


Figure 9. Transient Response of CG LNA.

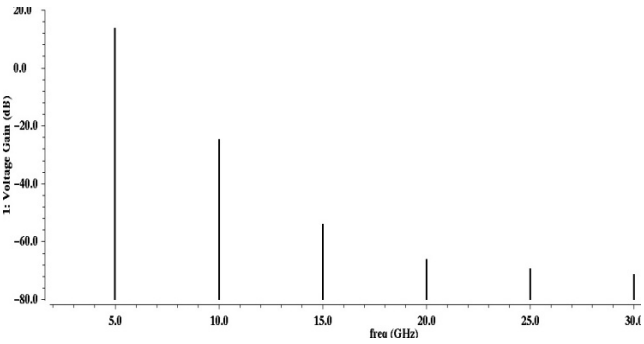


Figure 10. Voltage gain Vs frequency spectrum.

4.5 Power Gain

Power gain versus frequency response is shown in Figure 11. It is observed that the maximum power gain is obtained as 5.9 dB at operating frequency of 5 GHz and is goes decreasing as frequency increases.

4.6 S Parameter Analysis

S_{11} and S_{22} indicate input output return loss. It indicates how well the input impedance is matched with the

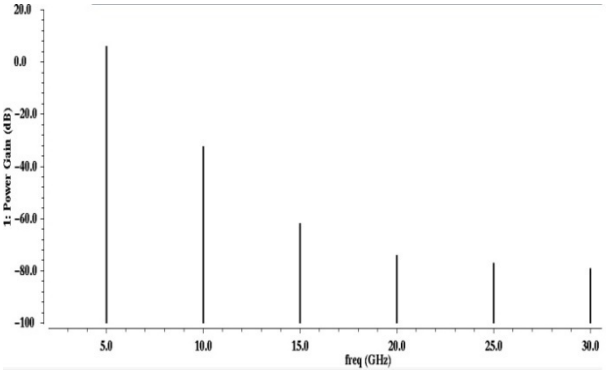


Figure 11. Power gain vs frequency spectrum.

reference input and output impedance is matched with the load impedance in a power transfer perspective. From Figure 12 S_{11} obtained as -12 dB and S_{22} is obtained as -17 dB.

Figure 13 shows the forward gain of the amplifier. The gain is observed is stable from 5 GHz range to 15 GHZ and the maximum value of gain is obtained as 17 dB at 5 GHz[30].

4.7 Stability Analysis

The simulation results for the stability factor versus frequency is shown in Figure 14. It is seen that the CG LNA explained here is unconditionaly stable, i.e., its stability factor K>1 at the operating fequency.The stability factor K is given by,

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta S|^2}{2|S_{21}S_{12}|} \geq 1 \qquad (12)$$

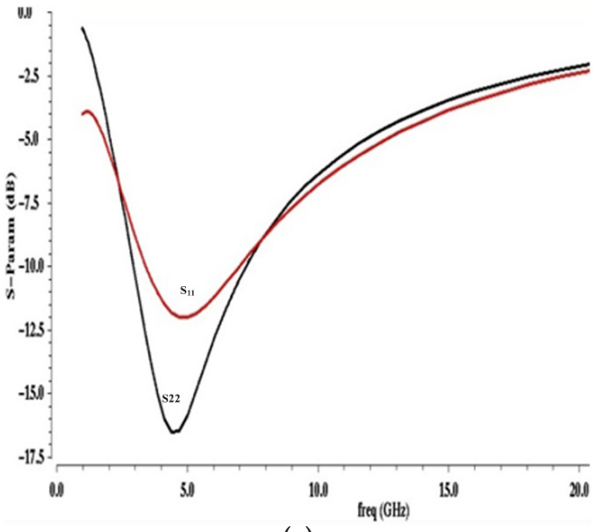
where the $|\Delta S| = |S_{11}S_{22} - S_{21}S_{12}|$

By substituting the values of $S_{11,}$ $S_{12,}$ $S_{21,}$ S_{22} it is observed that the K value is greater than 1.

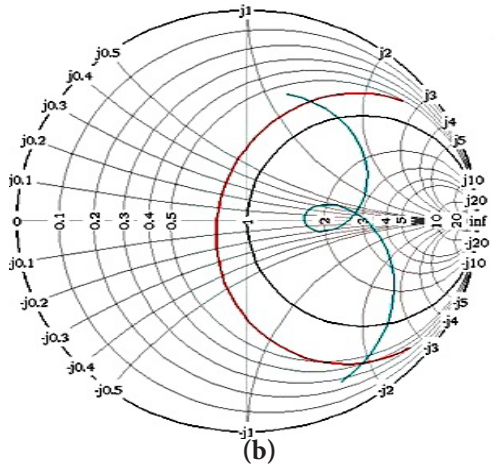
The effect of process temperature on stability is analyzed for the CG LNA. The temperature is varied from 20°C to 80°C. It is observed that there the device is stable over all these temperature range and the Kf value is greater than 1 in all these range. It is confirmed that the K_f value is not at all altered in these temparature range.

4.8 Linearity -1dB Compression Point and IIP3

Linearity measurments of LNA is explained in terms of 1 dB compression point and IIP3. The simulated 1 dB compression point at 5 GHz is calculated as -5.63 dB and IIP3



(a)



(b)

Figure 12. **(a)** S_{11} and S_{22} analysis. **(b)** Smith Chart Representation of S_{11} and S_{22} which are input and output reflection coefficients.

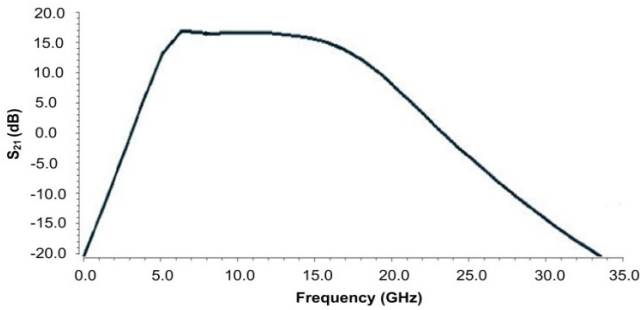


Figure 13. S_{21} –forward gain plot S_{21} value is obtained as maximum gain of 17 dB at a frequeny 5 GHz.

is obtaiend as 5.58 dB. By knowing either IP3 or P1 dB the other can be estimated[31] with the following rule-of-thumb formula and the value of P1 dB and IIP3 is verified. IIP3

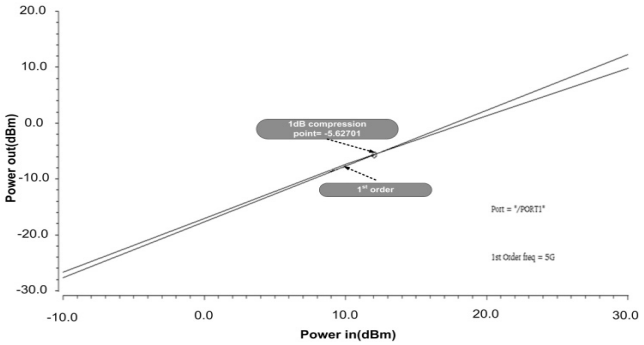


Figure 14. Temperature effect on stbility factor (K_f) vs frequency.

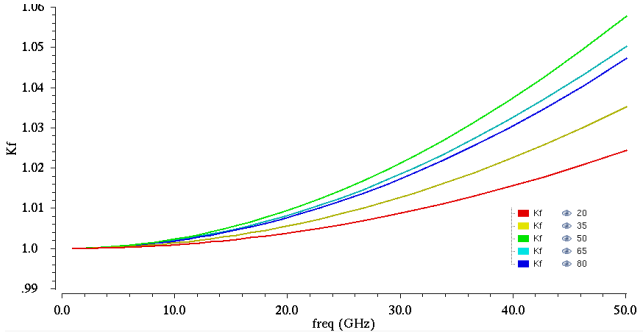


Figure 15. Input and output power with 1dB compression point.

Table 2. Comparison table of different LNA of 5 GHZ

References Nos.	Topology	Technology	F GHz	NF dB	Av dB `	S_{11} dB	S_{22} dB	P1dB dB	IIP3 dB	P_{dc} mw	A_p dB
18	Common Gate	0.18µm cmos	5.6	2.08	16.2	-39.6	-25.6	-	3.64	-	-
19	Common Source	0.18µm cmos	5	3.5	10	-16	-12	-5.3	4.9	7.2	-
20	Differential	0.180 TSMC	5.78	4.3	12.3	-11.8	-	0.3	3.8	4.98	-
21	Common Gate	0.18µm cmos	3.1-10.6	3.7-5.5	-	-9.6	-10	-	-13.1	3.1	-
22	Common Source	0.180 cmos	3-6.5	1.9-3.4	-	-12	-25	-	-13	4.5	-
25	Common Source	45nm MG-SiONFinFT	6	3.4	7.9	-8	-15	-	-	2.6	-
This work	Common Gate	30nm FinFET	5	1.26	17	-12	-17	-5.6	5.58	4.98	5.9

simulation performed on a very close frequency range of 5GHz and 4.65 GHz range.

$$IP3 = P1dB + 10dB \quad (13)$$

The IIP3 point allows the LNA to operate at a significant power level without any non-linear effects. The Figure 15 indicates the output referred IIP3. Table 1 and Table 2 shows the comparison of different parameters of designed FinFET CG LNA with recent 5 GHz LNA.The results shows that theNoise Figure obtained in this work is below 2 dB, which is less than all the previous work. Equation (7) shows the FinFET based CG LNA having a NF<2 dB. The power comparison shows the designed LNA having low power. Paper are FinFET based and the two works it gives better results in the aspects of noise figure, 1.26 dB. The value of noise figure maintains below 2 dB over a wide range of bandwidth by maintain the gain.

5. Conclusion

This works explains the performance of FinFET based CG LNA operating at 5 GHz. Performance characteristics have been compared with that of previously published LNA circuits operating at frequencies near to 5 GHz as shown in Table 2. It is observed that the designed FinFET LNA having better noise performance than the CMOS based LNAs. Here we are getting a low value of Noise Figure about 1.26 dB using FinFET, but in the case of

CMOS Common Gate LNA the noise figure greater than 2 dB. For a wide range of frequency 1.8 GHz to 26 GHz the noise Figure is observed below 2 dB. Noise Figure analysis for different capacitance and resistance modes are performed and the effect of parasitic capacitance and resistance are studied. Effect of temparature in noise figure and stbailty are also performed in CG LNA design and it is observed the design is thermaly stable and shows a less variation in noise figure over a temparature range of 20°C to 100°C. This work has also proved CG LNA gives a maximum voltage gain of 17 dB can be obtained which is a remarkable improvement compared to conventional CMOS LNA circuits without compromising the matching conditions and the rest of the performance metrics. The effect of thermal noise and flicker noise on noise figure also studied and it is concluded that the FinFET produce only thermal noise in the operating frequency range that is only about 8.47% of the total noise contribution of the whole amplifier.

6. References

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