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Investigation on cascade multilevel inverter with symmetric, asymmetric, hybrid and multi-cell configurations

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Abstract In recent past, numerous multilevel architectures came into existence. In this background, cascaded multilevel inverter (CMLI) is the promising structure. This type of multilevel inverters synthesizes a medium voltage output based on a series connection of power cells which use standard low-voltage component configurations. This characteristic allows one to achieve high-quality output voltage and current waveforms. However, when the number of levels increases switching components and the count of dc sources are also increased. This issue became a key motivation for the present paper. The present paper is devoted to investigate different types of CMLI which use less number of switching components and dc sources and finally proposed a new version of Multi-cell based CMLI. In order to verify the proposed topology, MATLAB – simulations and hardware verifications are carried out and results are presented.

1. Introduction

Plentiful industrial applications have begun to require higher power apparatus in recent years. Some medium voltage motor drives and utility applications require medium voltage and megawatt power level. For a medium voltage grid, it is difficult to connect only one power semiconductor switch directly. As a result, a multilevel power converter structure has been introduced as an alternative in high power and medium voltage situations. The concept of multilevel converters has been introduced since 1975. The term multilevel began with the three-level converter. Subsequently, several multilevel converter topologies have been developed.

There exist three commercial topologies of multilevel voltage-source inverters: neutral point clamped (NPC), cascaded H-bridge (CHB), and flying capacitors (FCs) [1–3]. Among these inverter topologies, CMLI reaches the higher

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Nomenclature

U_p	number of the dc voltage sources in the pth cell
K	number of cascaded sub multilevel cells
N_{level}	number of output voltage levels
$N_{\mathrm{IGBT},p}$	number of IGBTs used in pth cell
N_{IGBT}	the total number of IGBTs
$N_{\mathrm{switch},p}$	number of switches used in pth cell
$N_{\mathrm{switch},}$	the total number of switches
$V_{dc,p}$	the value of dc voltage sources in the pth cell
$V_{L,\max}$	maximum value of output voltage
$V_{\mathrm{std},p}$	sum of standing voltages on the switches of the pth cell
$V_{\mathrm{std,total}}$	total standing voltage on all of the switches used in the multilevel inverter
CF	cost function
$V_{\mathrm{switch,max}}$	the standing voltage of the highest –voltage switches
$V_{switch.\max}^{P.u}$	the standing voltage of the highest –voltage switches

output voltage and power levels (13.8 kV, 30 MVA) and the higher reliability due to its modular topology.

CHB multilevel inverters attain higher number of output voltage levels than twice the number of dc sources. Additionally, the series of H-bridges makes modularized layout and packaging. Although CHB multilevel inverters have good modularity they use higher number of switching components and dc sources [4–6]. This issue became a key motivation for the present paper. In the present paper different types of cascaded based multilevel inverters are investigated.

CHB type multilevel inverters can be operated in both symmetrical and asymmetrical configurations. While operating in symmetrical configuration, each H-bridge is supplied with finite DC source and the value of DC source is same for all H-Bridges. However, in this case each H-bridge will produce same output voltage (v, 0, and $-v$) by cascading such voltages multilevel waveform is produced. But, in order to generate high number of output levels, a large number of semiconductor devices and DC sources are required [7–10]. To overcome this problem, asymmetrical configurations came into existence. In asymmetrical configuration, each bridge is supplied with different DC sources and thereby each H-bridge gains the potential to generate different output voltages. By combining such voltages, increased number of levels is achieved in the output voltage [11,12].

In Asymmetrical configuration ratio of DC voltages for each H-bridge can be altered. For suppose if input voltages are changed in the ratio of 1:2 and 1:3 then inverters will produce seven level and eleven level output waveforms respectively. But in this configuration more than one H-bridge is essential to produce resultant waveform. However, asymmetrical configuration can also be obtained by changing the input voltages to H-bridge. In this case, only one H-bridge is sufficient. Thus, a large number of switching components are reduced in order to generate high number of output levels. Further, it is also possible to increase the number of levels in the output side by hybridizing the bridges. These classes of inverters are called hybrid inverters. In this case switching strategy plays a key role. Overall to generate large number of output levels with minimum switching components became a key aspect. Thus in the present paper different kinds of symmetrical, asymmetrical and hybrid configurations are presented. Finally, the MATLAB-simulation results are presented to verify the proposed topologies.

This paper is organized as follows. Section 2 shows the working principle of symmetric H-bridge topologies. Asymmetrical topologies for CHB inverters are presented in Section 3. In Section 4, Hybrid configurations of CHB inverters are introduced. Proposed multilevel inverter is introduced in Section 5 Comparative study is done in Section 6. Finally, conclusions are given in Section 7.

2. Symmetrical configurations of CHB inverter

Design shown in Fig. 1(a) is a series H-bridge inverter appeared in 1975, but a number of recent patents [13] have been obtained for this topology as well. Since this topology consists of series of power conversion cells, the voltage and power level may be easily scaled. Numerous advantages have been figured out using this topology, which are extensively used in medium and high power applications. Examining Fig. 1(b), the output phase voltage can be expressed as $v = v_1 + v_2 + v_3$, and this is because all the inverters are connected in series. Each single-phase full bridge inverter can generate three level outputs v_{dc}, 0 and $-v_{dc}$ and this is made possible by connecting the dc sources sequentially to the ac side via the four switching devices. Minimum harmonic distortion can be obtained by controlling the conducting angles at different inverter levels. Further, to improve the quality of the synthesized output waveform several PWMs are also available.

Thus, H-bridge configuration is quite renowned and gained popularity for its functions and features. To name some of the attributes of this converter, it is cost-effective, efficient, possible to modularize circuit layout and easy to pack, because each level has the same structure, and there are no extra clamping diodes or voltage balancing capacitors. However, CHB has a greatest disadvantage, i.e. it uses separate dc source for each H-bridge cell. Provision of separate dc source for each H-bridge cell, not only increases cost but also affects the reliability.

Further, to reduce the count of dc sources, CHB inverters are designed by employing single-phase transformers on the output side of H-Bridge is shown in Fig. 1(c). Although architecture is bulky in nature because of transformer it uses single DC source. Coming to operation point of view, structure has capacity to produce a seven level output voltage. Thus, performance is similar to that of conventional CHB seven level inverter. Later, simulation and FFT verifications are shown in Fig. 1(d) and (e).

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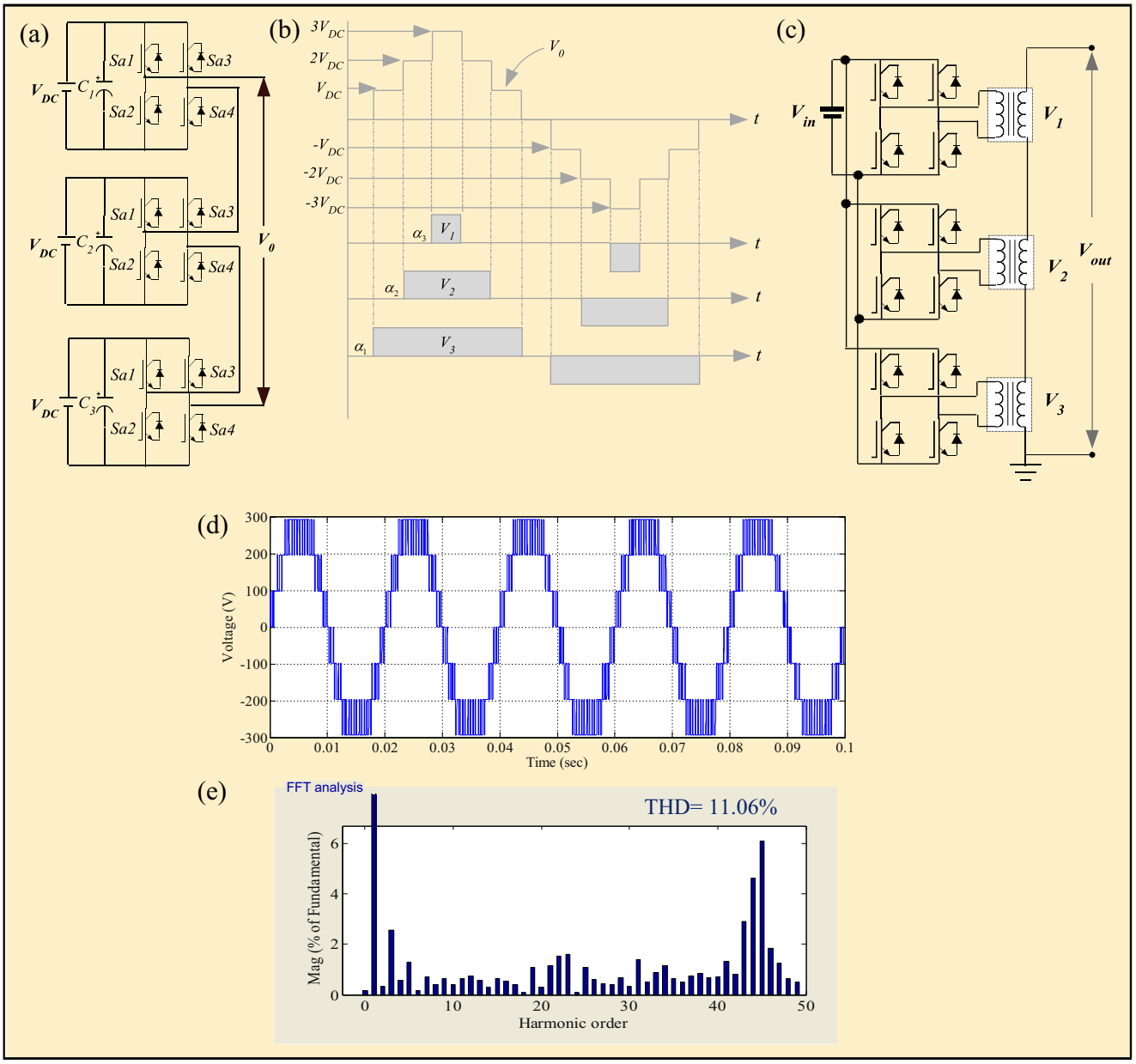

Figure 1 (a) CHB multilevel inverter, (b) key waveform for seven-level inverter, (c) CHB multilevel inverter by employing single-phase transformers, (d) simulation verification of seven-level CHB multilevel inverter, (e) FFT spectrum.

3. Asymmetrical configurations of CHB inverter

3.1. Asymmetrical configuration with symmetrical output voltages across each H-Bridges

The DC voltages of the H-bridge power cells introduced in the preceding section are all the same. Alternatively different dc voltages may be selected for the power cells [14]. Fig. 2(a) is constructed with unequal dc voltages, but of integer multiples magnitude dc sources. A switching scheme is implemented that renders an equal voltage stepped waveform. With $(m-1)/2$ number of dc sources m levels are achieved and $(m-1)$ numbers of odd harmonics are eliminated. Consequently, a number of sources required are halved.

Conversely, Fourier expansion of equal voltage steps is given by the following:

$$V(t) = \frac{4V_{dc}}{\pi} \sum_{n=odd}^{\infty} \cos n\theta \ \frac{\sin n\omega t}{n} \tag{1}$$

However, if voltage steps are unequal then,

$$V(t) = \frac{4V_{dc}}{\pi} \sum_{n=odd}^{\infty} \sum_{j-1}^{m-1} V_j \cos n\theta_n \ \frac{\sin n\omega t}{n} \tag{2}$$

where V_j are the least common factor of voltages. On the other hand, if the voltages are integer multiples then above equation can be written as

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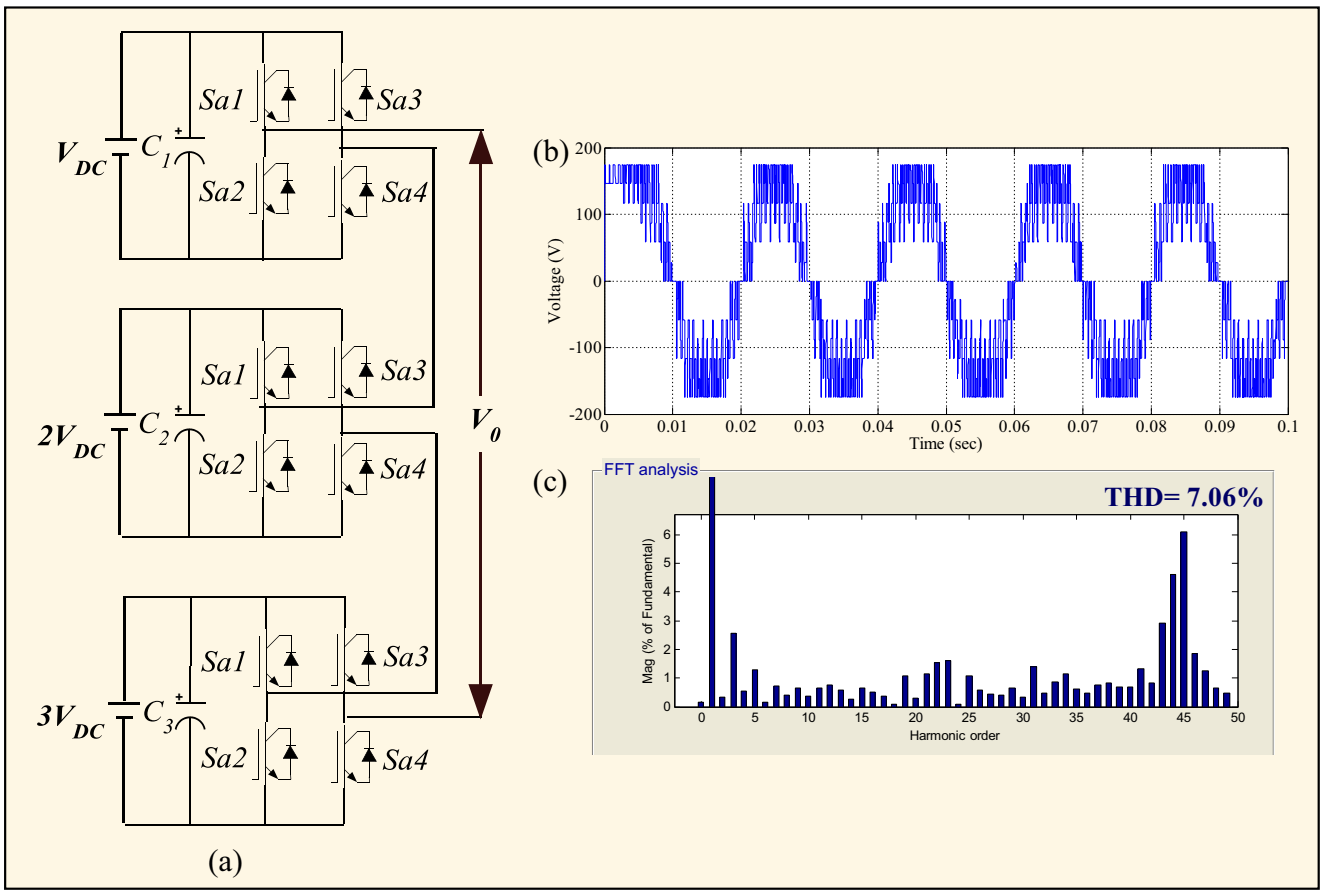

Figure 2 (a) Asymmetrical thirteen-level CHB inverter, (b) simulation verification of thirteen-level CHB multilevel inverter, (c) FFT spectrum.

$$V(t) = \frac{4V_{dc}}{\pi} \sum_{n=odd}^{\infty} \sum_{j-1}^{m-1} j \cos n\theta_n \frac{\sin n\omega t}{n} \tag{3}$$

Equation is solved for the values of θ_n.

Thus, with the help of switching scheme, a number of voltage levels can be increased without necessarily increasing the number of H-bridge cells in cascade. This permits more voltage steps in the inverter and thereby yields improved voltage waveform for the same number of power cells. In the present structure the dc voltages for *H-bridges* are chosen as V_{DC}, 2 V_{DC}, and 3 V_{DC} respectively. The three-cell inverter leg is able to produce thirteen level voltage waveform; that is, voltage waveform constitutes $6V_{DC}$, 5 V_{DC}, 4 V_{DC}, 3 V_{DC}, 2 V_{DC}, V_{DC}, 0, $-V_{DC}$, -2 V_{DC}, -3 V_{DC}, -4 V_{DC}, -5 V_{DC}, and -6 V_{DC}. Simulation and FFT results are shown in Fig. 2(b) and (c)

3.2. Asymmetrical configurations with asymmetrical output voltages

In preceding section, asymmetrical configuration is introduced, but output voltages produced across each H-bridge are in symmetric in nature. It is also possible to develop an asymmetric configuration with asymmetrical output voltages. This control strategy allows us to generate large number of output levels. Fig. 3(a) illustrates asymmetrical 27-level inverter using H-bridges. As shown, the dc power supplies of each one of the three inverters are isolated and need to be bidirectional. Besides, the dc supplies are scaled with levels of voltage in power of three. The scaling of voltages in power of three allows having, with only three inverters, $3^3 = 27$ different levels of voltage: 13 levels of positive values, 13 levels of negative values, and zero. The inverter positioned at the top of the figure has the largest voltage, and will be called main inverter. Remaining two modules will be the auxiliary inverters. The most important mechanism at a lower switching frequency carries more than 80% of the total power, which is an additional benefit of this architecture for high-power applications.

More than 80% of the power is delivered by the main inverter, about 15% for the Aux-1 inverter, and less than 4% of the total power for Aux-2 inverter. Despite Aux inverters need low-power sources they have to be bidirectional. To overcome this issue three solutions are recommended: (1) active front-end rectifiers; (2) bidirectional dc–dc power supplies; and (3) passive rectifiers with dissipative resistors. Although negative power exists at certain levels of voltage, simple unidirectional rectifiers and special PWM techniques could be applied. This PWM is based on jumping some voltage levels when average power in a period becomes negative. This technique works well for both Aux-1 and Aux-2 inverters. However, the structure for the small Aux-2 inverters can be simplified by means of suitable PWM technique. In the case of Aux-2, the power transfer is even smaller (less than 4%), and it can be managed to keep average power to zero by using floating capacitors and a particular PWM techniques, but keeping THD as low as possible.

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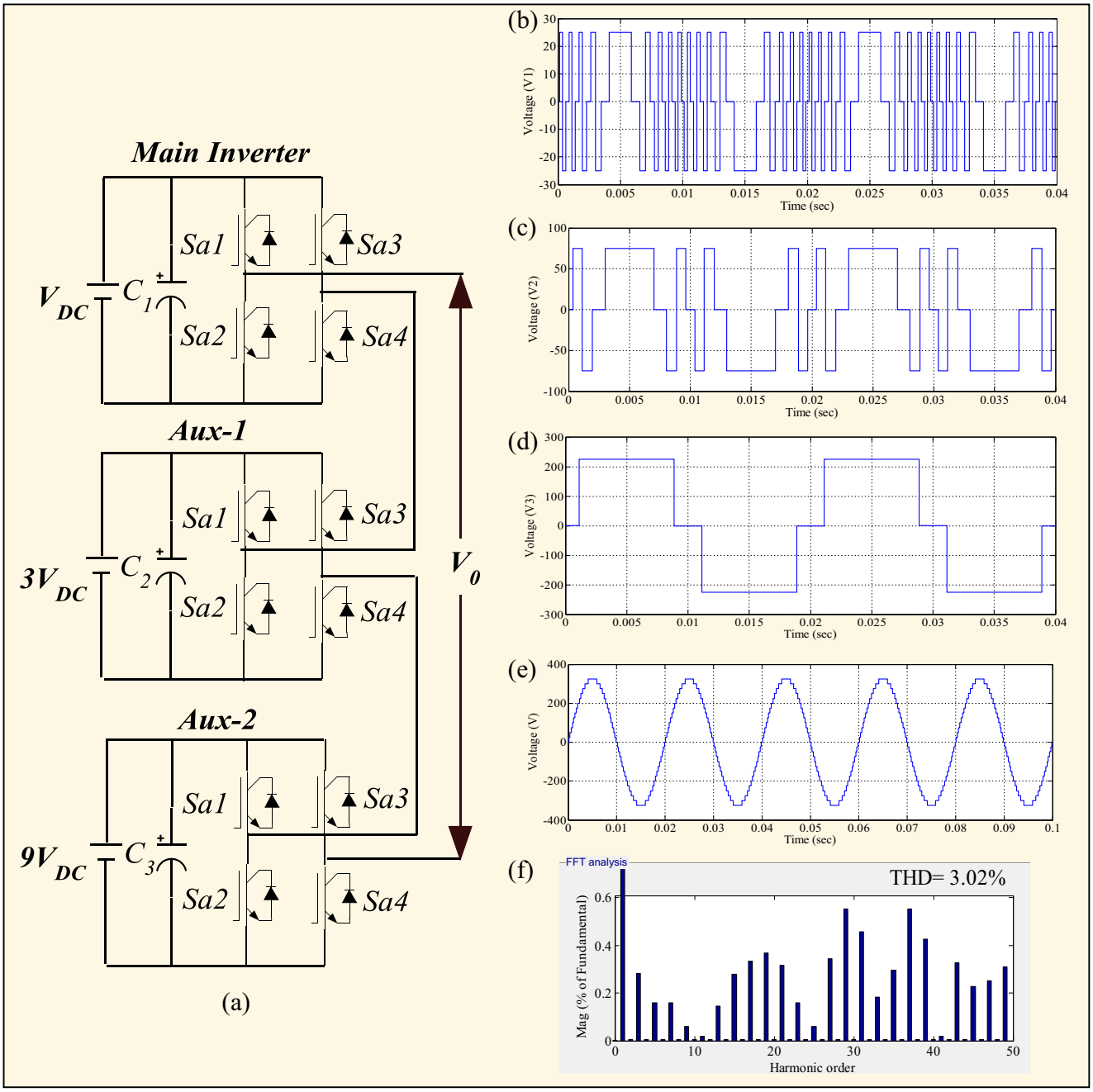

Figure 3 (a) Asymmetrical CHB multilevel inverter, (b) output voltages of each H-bridge module, (c) twenty-seven level output voltage waveform, (d) FFT spectrum.

Fig. 3(b) demonstrates the simulation verifications of the asymmetrical cascade multilevel inverter and each H-bridge produces 25, 75 and 225 volts respectively. Further. Fig. 3(c) shows the 27 level output voltage which is resultant of three H-bridges. FFT spectrum for output voltage is exposed in Fig. 3(d). Observing FFT spectrum, lower order harmonics are absolutely minimized and THD produced is 3.02%.

3.3. CHB based asymmetrical configurations by using sub-cells

Fig. 4(a) shows the basic unit for a sub-multilevel inverter. This consists of a dc voltage equal to V_{DC}, with two switches S_1 and S_2. Table 1 indicates the values of V_0 for states of switches S_{11} and S_{12}. It is obvious that both switches S_{11} and S_{12} cannot be ON simultaneously because a short circuit across the voltage V_{DC} would be produced. It is noticed that two values can be achieved for V_0. The sub cell can be cascaded as shown in Fig. 4(a). Although this topology requires multiple dc sources, in some systems they may be available through renewable energy sources such as photovoltaic panels or fuel cells or with energy storage devices such as capacitors or batteries. When ac voltage is already available, multiple dc sources can be generated using isolated transformers and rectifiers. The output voltage of the sub-cell inverter is sum of

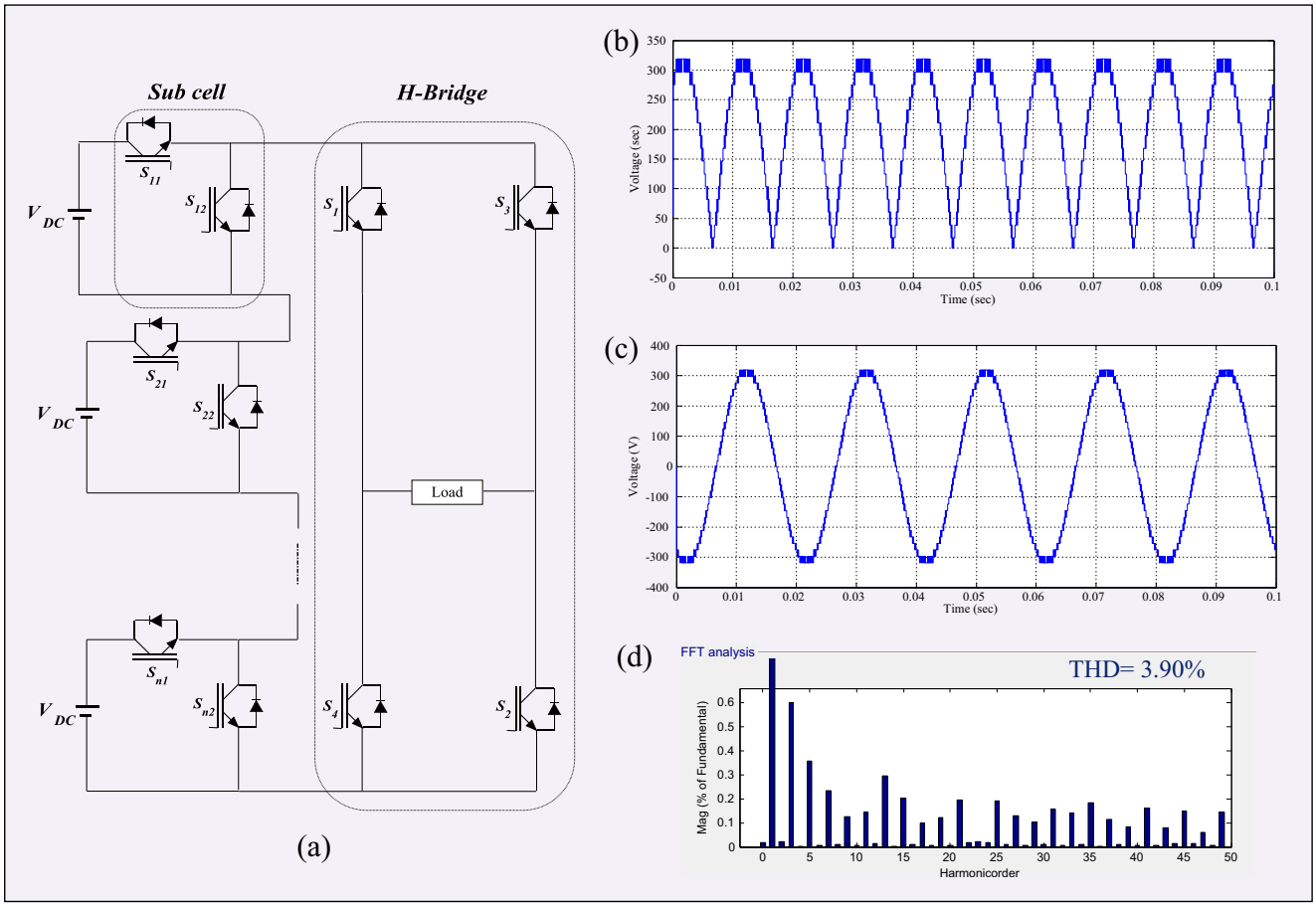

Figure 4 (a) Asymmetrical CHB multilevel inverter using sub-cells, (b) output voltage of sub-cells, (c) thirty-one level output voltage waveform, (d) FFT spectrum.

Table 1 Switching operation.

State	S_{11}	S_{12}	V_O
1	On	Off	V_{dc}
2	Off	On	0

the outputs of all individual sub cells shown in Fig. 4(b) and herein this output is fed to the standard H-bridge. To get the resultant level across the load, a number of sub-cell input need to been taken into account. For example, to attain a five level output waveform design should constitute three sub-cells.

The proposed multi-cell CMLI is simulated in MATLAB-simulink. Fig. 4(c) shows a 31-level multilevel inverter and can generate staircase waveform with maximum 320 V on output. The load is a series R–L with magnitudes 100 Ω and 50 mH, respectively. There are several modulation strategies for multilevel inverters [15]. In this work, sine triangle PWM modulation is carried out for sub-cells. The important point in switching criterion is, only sub cell is switched in PWM mode, whereas H-bridge is operated in normal switching mode. This benefit reduces the switching losses in the main H-bridge module. But, the voltage ratings of switching components of standard H-bridge need to be very high. Further, FFT spectrum shown in Fig. 4(d) exemplifies reduction in lower order harmonics and output voltage waveform is quite smooth in nature.

4. Hybrid configurations of CHB inverter

4.1. Hybrid configuration of CHB inverter using H-bridges

Fig. 5(a) demonstrates the Hybrid CHB and its operation. This class of inverter is highly visible in grid connected/Photo voltaic systems. Authors [16] have finite contributions regarding this archetype. On inspecting the architecture, one H-bridge module is operated in PWM mode and others are operated in fundamental switching mode. Thus, this kind of switching strategy results in minimization of switching losses. In fact there are huge control approaches based on this switching logic. But in all the cases fundamental principle is same. For better understanding simulation verification and FFT report of output voltage are exposed in Fig. 5(b) and (c) of Hybrid CHB multilevel inverter.

Observing keenly, eleven-level output could be predicted in the output voltage waveform. At this point readers should observe that, terminal voltages of bridge 2 and 3 are fundamental voltages and terminal voltage for bridge 1 is PWM voltage. Combining all such voltages produces a resultant waveform. This is an efficient technique to increase the output levels. But at the same moment its greatest limitation is

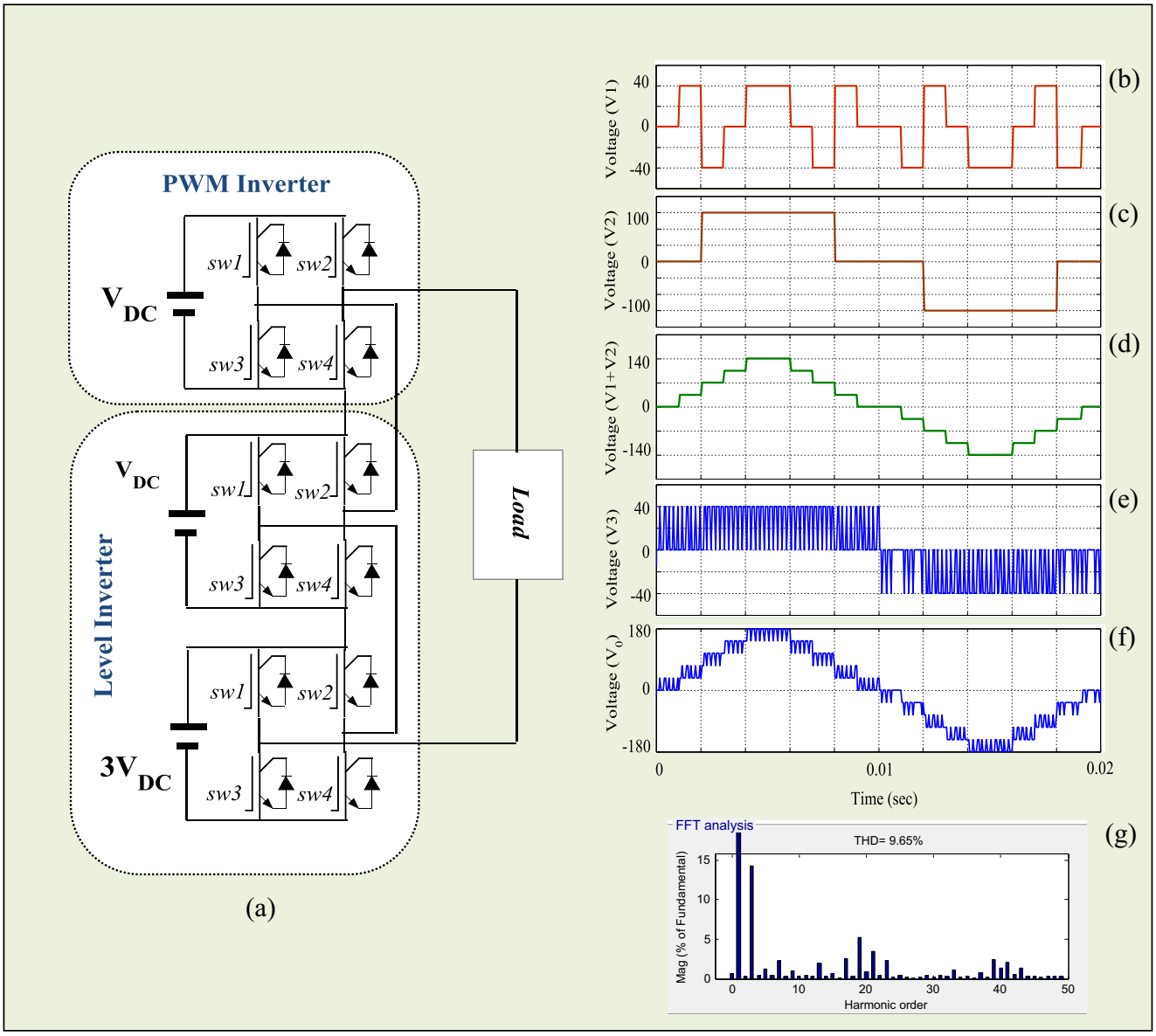

Figure 5 (a) Hybrid CHB multilevel inverter, (b) output voltage of each H-bridge and load voltage (nine-level) waveform, (c) FFT spectrum.

complexity in switching scheme and the presence of third harmonic component.

4.2. Hybrid configurations of CHB inverter using H-bridge and three-phase traditional inverter

Hybrid multilevel inverter using traditional inverter is shown in Fig. 6(a), which includes complete three-phase architecture. The bottom is one of a standard 3-leg inverters with a dc power source. The top is an H-bridge in series with each standard inverter leg [17–19]. The H-bridge can use a capacitor, battery or other dc power source. The output voltage v_1 of this leg (with reference to the ground) is either $+Vdc/2$ (S5 closed) or $-Vdc/2$ (S6 closed). This leg is allied in series with a full H-bridge, which in turn is provided by a capacitor voltage. If the capacitor is used and kept charged to $Vdc/2$, then the output voltage of the H-bridge can take on the values $+Vdc/2$ (S1, S4 closed), 0 (S1, S2 closed or S3, S4 closed), or $-Vdc/2$ (S2, S3 closed). The capacitor's voltage regulation control method consists of, monitoring the output current and the capacitor voltage, during periods of zero voltage output, either the switches S1, S4, and S6 are closed or the switches S2, S3, and S5 are closed, depending on whether it is necessary to charge or discharge the capacitor. The method followed here depends on the voltage and current not being in phase. It represents that either positive or negative current is needed when the voltage is passing through zero in order to charge or discharge the capacitor. Consequently, the amount of capacitor voltage in this scheme can regulate depends on the phase angle difference of output voltage and current. One of the critical issues in this topology is charging and discharging of a capacitor and it entirely depends on the modulation index. However, in the present case, performance verification is carried out with level shifted PWM. The simulation and FFT verifications are

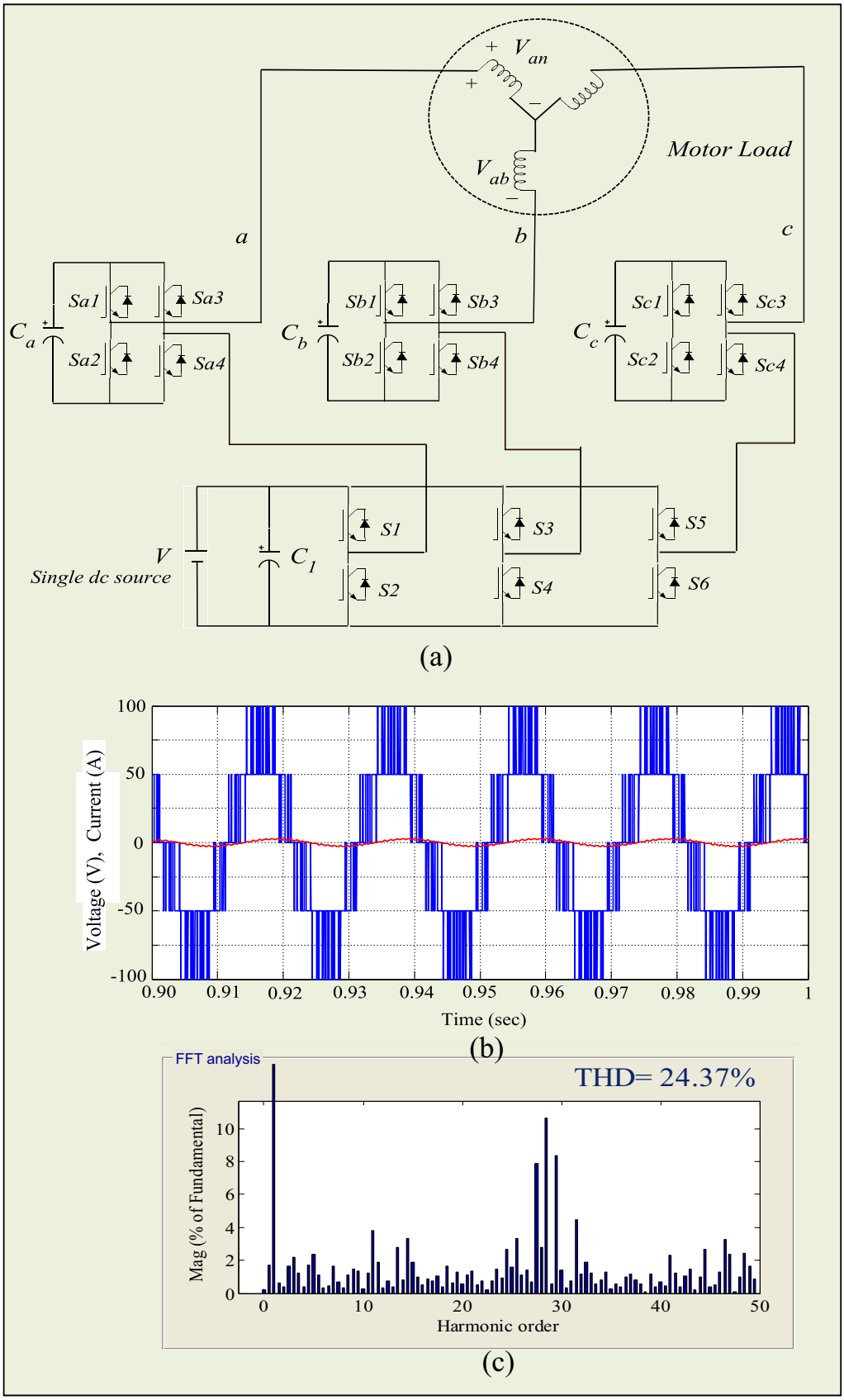

Figure 6 (a) Hybrid multilevel inverter using traditional inverter, (b) output voltage waveform, (c) FFT Spectrum.

presented in Fig. 6(b) and (c) respectively. Examining, performance of inverter is flexible. FFT spectrum specifies reduction in lower order harmonics. However as modulation index decreases odd harmonic components are significantly noticed. In fact, these classes of inverters are widely used in utility interface applications with renewable energy source due to its functions and features. In common the hybrid cascaded H-bridge multilevel inverters are adapted for solar grid application, because the bottom standard 3-leg inverter connects with a solar panel and the top three H-bridges use a battery separately as an energy storage device.

5. Proposed CMLI using sub-multi cells

5.1. Proposed asymmetrical multi-cell CMLI

The proposed asymmetrical multi-cell CMLI consists of n equal non-isolated dc voltage sources which are used to synthesize a multilevel output voltage by means of power electronic switches. The switches used in the topology are of two types. Some of them have to block both positive and negative voltages and conduct the current in both directions. Therefore, these switches must be bidirectional. The other switches have to withstand voltage only with a specific polarity so that they are unidirectional. When a number of dc sources per each basic cell (n) = 1, 2 then unidirectional switches are sufficient to perform the operation of proposed topology. But if $n \geqslant 3$ then bidirectional switches need to be incorporated. Fig. 7 shows the multi-cell configuration have only unidirectional switches since each sub-multi cell consists merely of two dc sources. Although the proposed configuration can be extended to any number of voltage levels, the switches T_1–T_4 have to withstand a voltage equal to the total dc voltage. This promotes to cascade the multi-cells so that the voltage is shared between the switches making it suitable for higher voltage applications, and the proposed sub-multilevel cells generates the output voltage of 2 N + 1 levels.

In the asymmetric multilevel inverter the value of the dc voltage sources used in the different cells is assumed to be different so that more output voltage levels can be generated using fewer switching devices. Suppose that the pth cell has u_p equal dc voltage sources and consider the value of the first cell dc voltage sources to be as follows

$$V_{dc}, 1 = V_{dc} \tag{4}$$

Then, the value of each dc voltage source of the pth cell can be determined as follows:

$$\begin{aligned} V_{dc,p} &= (2u_1 + 1) \cdot (2u_2 + 1) \ldots (2u_p - 1 + 1) V_d \\ &= V_d \cdot \prod_{n=1}^{p-1} 2u_n + 1 \end{aligned} \tag{5}$$

The values of the dc voltage sources of the cells are determined in way that the number of output voltage levels is maximized. With the values given in (2) for the dc voltage sources, the number of output voltage levels can be obtained as follows:

$$\begin{aligned} N_{leel} &= [(2u_1 + 1) \cdot (2u_2 + 1) \ldots (2u_k + 1)]. \\ &= \prod_{n=1}^{k} 2u_n + 1 \end{aligned} \tag{6}$$

The maximum value of the output voltage can be written as

$$\begin{aligned} V_{L,\max} &= \frac{[(2u_1 + 1) \cdot (2u_2 + 1) \ldots (2u_k + 1)] - 1}{2} \cdot V_d \\ &= \frac{\left[\prod_{n=1}^{k} (2u_n + 1)\right] - 1}{2} \cdot V_d \end{aligned} \tag{7}$$

The number of switches and IGBTs used in the proposed multi-level inverter can be calculated by the following equations.

$$N_{\mathrm{IGBT},p} = 2(u_p + 1) \tag{8}$$

$$N_{\mathrm{IGBT}} = \sum_{n=1}^{k} (2u_n + 1) \tag{9}$$

The standing voltage on the switches of the pth cell is the same as stated by

$$V_{\mathrm{std}} = \begin{cases} \left(\frac{3u^2+2u-5}{8} + 4u\right) V_{dc,p} & \text{for } u: \ odd, \frac{u-1}{2} : een \\ \left(\frac{3u^2+2u-1}{8} + 4u\right) V_{dc,p} & \text{for } u : odd, \frac{u-1}{2} : odd \\ \left(\frac{3u^2+2u}{8} + 4u\right) V_{dc,p} & \text{for } u : odd, \frac{u-1}{2} : odd \end{cases} \tag{10}$$

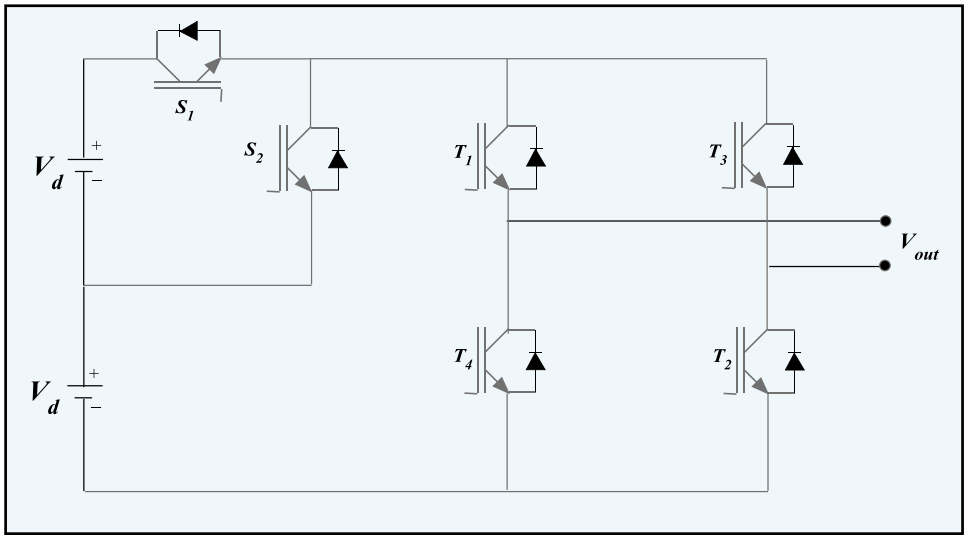

Figure 7 The proposed multi-cell CMLI.

Total standing voltage on all of the switches of the proposed asymmetric CMLI can be written as follows

$$V_{\text{stdf}} = \sum_{p=1}^{k} V_{\text{std},p} \tag{11}$$

Fig. 8(a) shows a 25 level asymmetric inverter based on proposed topology, and the values of the dc voltage sources have been in order to get the maximum output voltage of 312 V (220 V rms voltage). Further, Fig. 8(b) presents the details of voltage waveforms across each H-bridge. Observing the waveforms, output of first sub cell multilevel inverter is in asymmetric in fashion which produces maximum voltage of 52 V. Later on, second H-bridge produces a square wave output of 260 V dc. Finally, combining two H-bridge voltages we obtain a resultant voltage which constitutes 25-Levels in the output voltage (312 V). The corresponding switching table of proposed topology is mentioned in Table 3.

5.2. Simulation and hardware implementation of proposed multilevel inverter

The desired output voltage waveform is generated with the aid of MATLAB/Simulink software by simulation. The multilevel shown in Fig. 8(a) is a 25-level multilevel inverter and can generate staircase waveform with maximum of 220 V RMS in output. The load is a series R–L with magnitudes 70 Ω and 55 mH, respectively. To control the proposed multilevel inverter the stair case control technique is adopted. In this control technique, at any instant of time the nearest level with reference output voltage is chosen. This approach is known as nearest level or round control technique. By adopting this method, we can achieve stair case voltage which has a minimum error with respect to reference voltage. Further, simulation results are presented in Fig. 9. By observing the verifications, Fig. 9 (a) and (b) presents the details of output voltage across each H-bridge. Fig. 9(c) presents the details of resultant output voltage across load. The stepped output voltage waveform of the multilevel inverter is combination of fundamental frequency sine wave components and a myriad number of odd harmonic components. The desired output can be produced with increase in number of the voltage steps.

Table 2 Hardware specifications.

Items	Specifications and features
Switching devices	IGBTCM100DU12H, 600 V, 100 A MITSUBISHI IGBT MODULES
Input voltage	100 V, 4-DC Sources
Output voltage	25 level, 50Vac, 50 Hz
DSP	eZdspTMF28335
Load parameters	R = 70 Ω and L = 55 mH

To verify the simulation results, prototype setup for proposed asymmetric cascaded MLI is demonstrated in Fig. 10. Further, for the experimentation DSP based module was used to generate the required gate pulses. To program the DSP, two distinct software packages are used in MATLAB and code composer studio. DSP is connected to MATLAB by a USB JTAG controller which establishes connection between DSP and MATLAB. In MATLAB the program is written and dumped into DSP to generate the required gate signals.

Total two H-bridge modules and two sub-multi cells are used. The measured quantities are the stepped DC voltages,

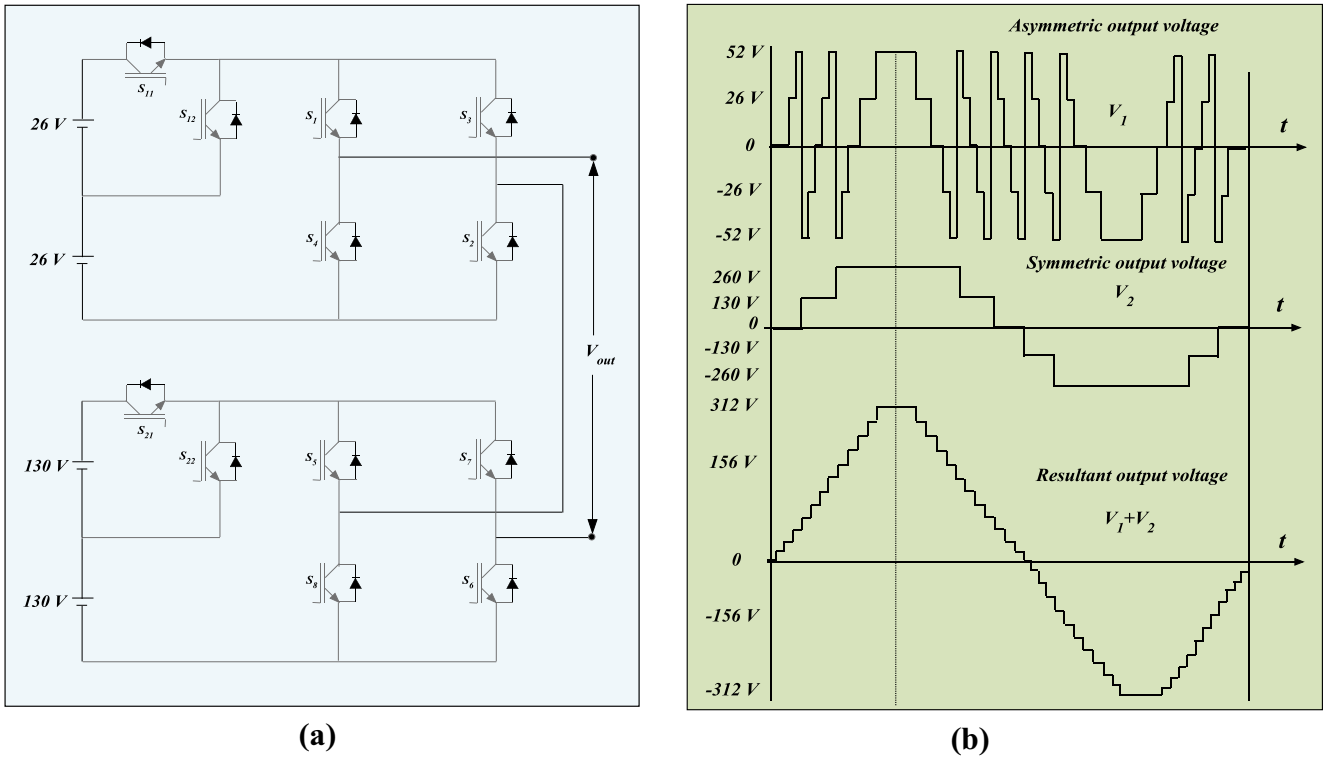

Figure 8 (a) The proposed 25-level asymmetric multi-cell CMLI, (b) key waveforms.

Table 3 Switching table for proposed topology.

Level	S1	S2	T1	T2	T3	T4	S3	S4	P1	P2	P3	P4
0	0	0	1	0	1	0	0	0	1	0	1	0
1	0	0	1	1	0	0	0	0	1	0	1	0
2	1	0	1	1	0	0	0	0	1	0	1	0
3	1	0	0	0	1	1	0	0	1	1	0	0
4	0	1	0	0	1	1	0	0	1	1	0	0
5	0	0	1	0	1	0	0	0	1	1	0	0
6	0	0	1	1	0	0	0	0	1	1	0	0
7	1	0	1	1	0	0	0	0	1	1	0	0
8	1	0	0	0	1	1	1	0	1	1	0	0
9	1	0	0	0	1	1	1	0	1	1	0	0
10	0	0	1	0	1	0	1	0	1	1	0	0
11	0	0	1	1	0	0	1	0	1	1	0	0
12	1	0	1	1	0	0	1	0	1	1	0	0

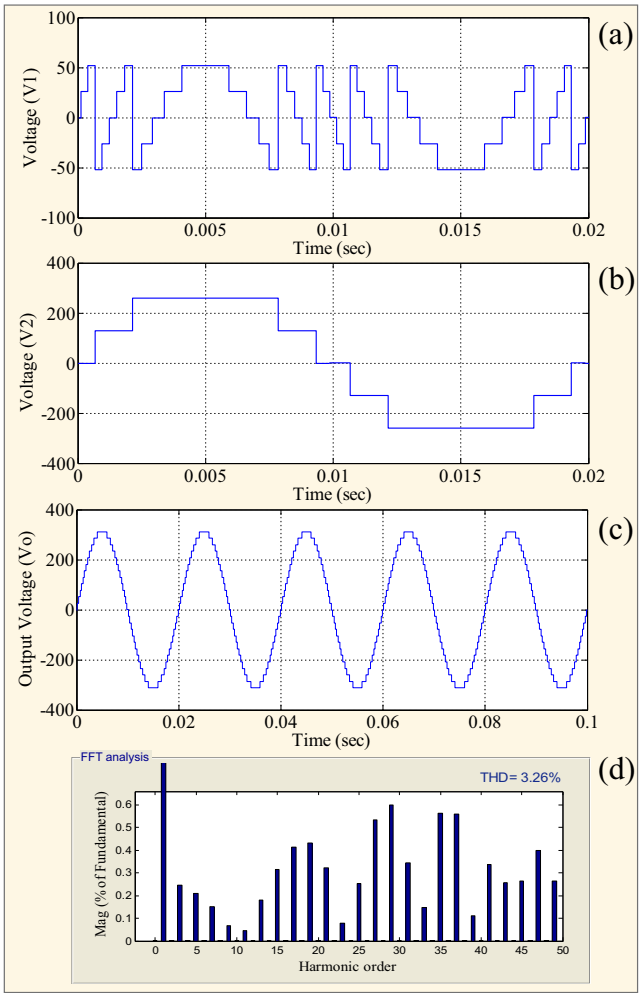

Figure 9 (a) Output voltage of first H-bridge, (b) output voltage of second H-bridge, (c) resultant output voltage with 25-levels, (d) FFT spectrum.

load voltages. With the help of DSP, gate signals are generated. Target output voltage and its frequency are 312 V Ac and 50 Hz respectively. For experimentation highly inductive

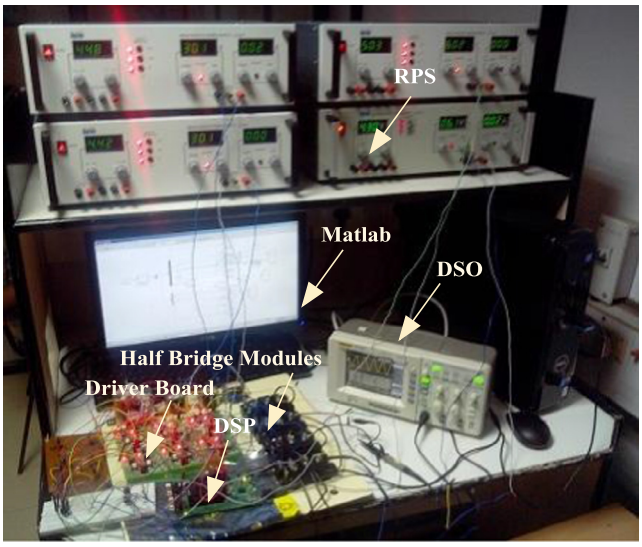

Figure 10 Details of hardware setup.

load is considered. Detailed component list is given in Table 2. Further Fig. 11 presents the details of hardware result. Results are extracted similar to those of simulation. It's clear that, voltage from output voltage (v_1) and output voltage (v_2) exactly matches with the simulation verifications. Further slight notch is observed in the voltage (v_1), and this is due to sharp switching. This can be evaded by appropriate switching method. Further, it can be evident that output voltage (with 25-levels) is quite smoother and almost reaches to sine waveform. FFT spectrum in Fig. 11(d) presents the harmonic details. Observing spectrum, dominant harmonics such as 3, 5, 11, and 13 are having 0.72%, 0.31%, 0.42% and 0.2% of harmonic distortions in the output voltage respectively. THD is about 3.6%. In fact the proposed architectures are well designed with less number of switching components with appropriate switching, in order to achieve high quality output voltage. Further, in application point of view this topology would be appropriate to power generation, energy transmission and power quality devices (DVR, D-STATCOM, Active power filter, Unified power quality conditioner).

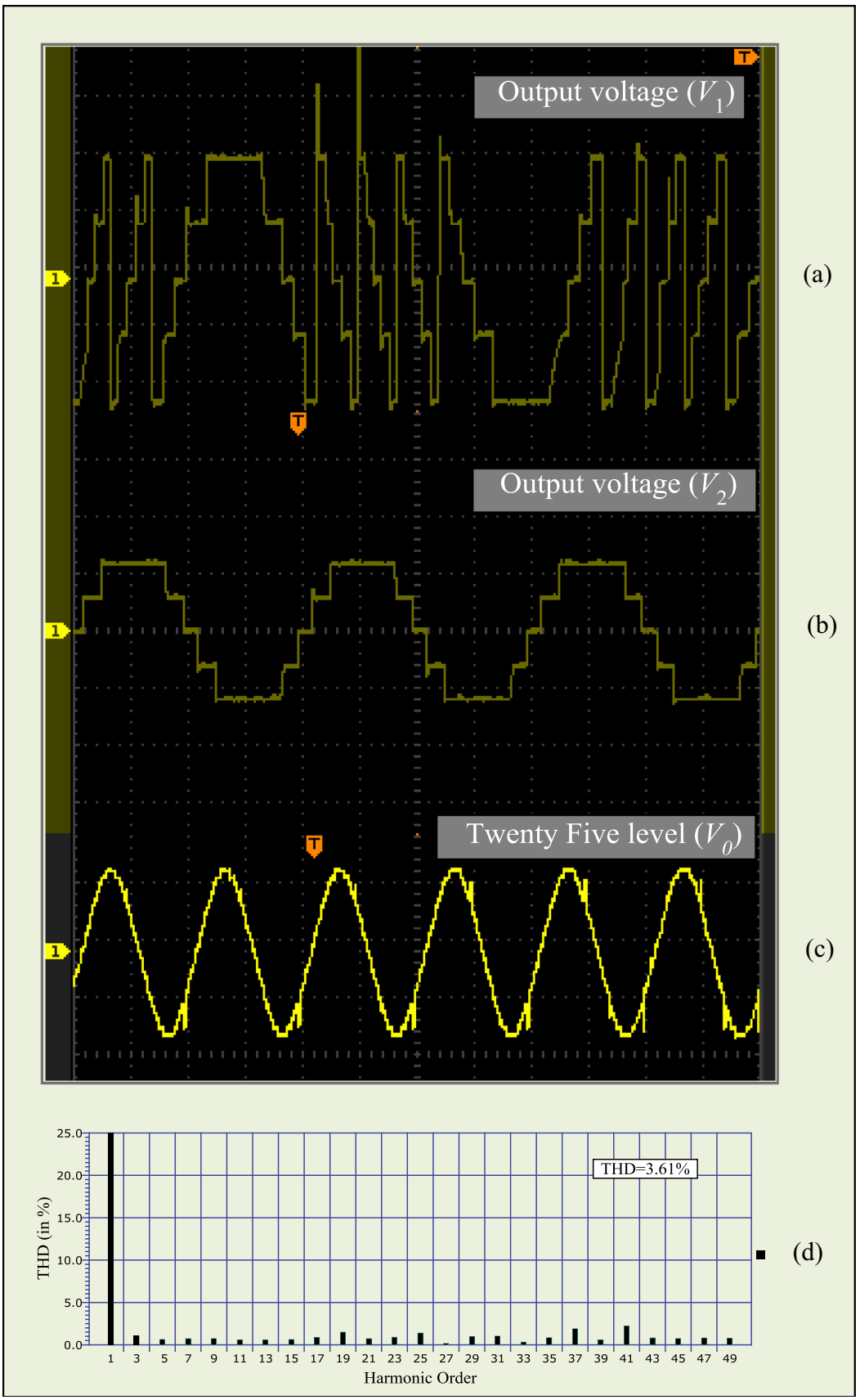

Figure 11 (a) Output voltage of first H-bridge (V1), (b) output voltage of second H-bridge (V2), (c) resultant output voltage with 25-levels (V0), (d) FFT Spectrum for output voltage (25-levels).

Table 4 Component comparison.

Items	Switch	Clamping diode	Balancing capacitors	DC-bus
Diode clamped	48	870	NA	24
Flying capacitor	48	NA	435	24
Cascade multilevel inverter	48	NA	NA	12
Asymmetrical CMLI with symmetrical outputs	26	NA	NA	8
Asymmetrical CMLI with asymmetrical outputs	14	NA	NA	4
Asymmetrical CMLI by using Sub-Cells	36	NA	NA	16
Hybrid CMLI using only H-bridges	16	NA	NA	4
Proposed multi-cell based CMLI	12	NA	NA	4

6. Comparative study

To confirm the merits and demerits of proposed architectures a small comparison is done among the former and proposed multilevel inverter. Table 4 articulates the comparative study, and herein comparative approach is done with NPC, FC and CMI based inverter. In general to produce a 25-level phase voltage from an NPC, FC and CMI require at least 48 semiconductor switches [8]. On the other hand, in asymmetrical and hybrid CHB multilevel inverters with both symmetric and asymmetric output voltages require 26 and 14 switches respectively. Further, like NPC and FC extra clamping diodes and balancing capacitor are not required. Another remarkable issue is DC-Bus count; it is only 4 DC sources are required for the proposed inverter to generate 25 level output waveform, whereas in traditional cases it is 24, 24 and 12 for NPC, FC and CMI respectively. Furthermore, larger number of dc sources are required for asymmetrical and hybrid configurations. Thus from this comparison we can conclude that, proposed configuration uses less number of switching components to produce same number of output levels.

7. Conclusion

In this paper CMLI with sub-cells is proposed with less number of switches. To highlight the merits of proposed inverter, an in-depth investigation is carried out on symmetric, asymmetric and hybrid multilevel inverters based on CHB topologies. Symmetric configuration has capacity to produce only limited number of levels in output voltage. On the counter side, symmetrical configuration can be operated in asymmetrical mode with different DC sources. However, asymmetrical configurations can produce higher number of output levels and thereby qualitative output waveforms could be generated. Later, hybrid CHB inverters are also introduced, which utilizes single DC source for entire structure. Thus complexity and voltage balancing issues can be reduced. Finally proposed inverter is introduced with less number of switching components and able to produce qualitative output waveforms. To verify the proposed inverter adequate simulation is done with help of MATLAB simulink. Later on, hardware variations are carried out in laboratory. Verifications are quite impressive with greater number of levels in the output voltage and lower harmonic content in FFT spectrums. Spectrums indicate that, low order harmonics are drastically reduced. Thus power quality is significantly enhanced. Thus proposed inverter shows some promising attributes when compared with traditional CHB based architectures.

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